IN THE CLAIMS:

Please amend the claims as follows.

1-12 (Canceled)

13. (Previously Presented) A method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level, said first wiring patterns being connected to a gate electrode on a gate insulating film formed on a semiconductor region, and said second wiring pattern being connected to said semiconductor region, wherein in patterning said first and second wiring patterns, a dummy wiring pattern electrically separated from and placed between said first and second wiring patterns on said same level is left unetched, the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

14. (Previously Presented) A method according to claim 13, wherein the spaces between said dummy pattern and said first, and second wiring patterns are set generally equal to a minimum pattern space of said first, and second wiring patterns.

15. (Canceled)

16. (Previously Presented) A method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level, said first wiring patterns each being connected to a gate electrode on a gate insulating film formed on a semiconductor region, and said second wiring pattern

being connected to said semiconductor region, wherein in patterning said first and second wiring patterns, at least one dummy wiring pattern which is electrically separated from and placed between said first and second wiring patterns on said same level is left unetched, the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

17. (Previously Presented) A method according to claim 16, wherein the spaces between each adjacent pair of wiring patterns are set equal to a minimum wiring pattern space of said first and second wiring patterns.

18. (Previously Presented) A method according to claim 16, further comprising a third wiring pattern between said first wiring pattern and said second wiring pattern, the third wiring pattern being connected in the circuit of the semiconductor device, wherein said at least one dummy wiring pattern includes at least one dummy wiring pattern in each of the spaces between said third wiring pattern and said first and second wiring patterns.

19. (Previously Presented) A method according to claim 18, wherein the spaces between each adjacent pair of wiring patterns are set equal to a minimum wiring pattern space of said first and second wiring patterns.